



BAA97-38 VLSI Photonics

VCSEL-Based Interconnects in VLSI Architectures for Computational Enhancement



VIVACE

DARPA/MTO Review

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- | | |
|---|---|
| <ul style="list-style-type: none">• Honeywell Laboratories (lead)• Honeywell VCSEL Products Division• Honeywell Space Systems• Applied Photonics, Inc.• University of Delaware• Boeing Defense & Space Group• Defense Group, Inc.• George Mason University• MicroFab Technologies, Inc.• CFD Research Corp.• <i>Sun MicroSystems, Inc.</i>• <i>Intel Corp.</i> | <p>Minneapolis, MN Plymouth, MN / Richardson, TX Clearwater, FL Fairfax, VA Wilmington, DE Seal Beach, CA Santa Monica, CA Fairfax, VA Plano, TX Huntsville, AL <i>Mountain View, CA</i> <i>Hillsboro, OR</i></p> |
|---|---|

*vivace, adv. or adj. (lt.), vivacious; in a brisk spirited manner

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VIVACE Program Objective



Perform a system demonstration of a stressing military application (satellite-based HSI) using MPI as an application communication interface on a distributed, multiprocessor system composed of COTS processors.

Provide data communication in the network via fiber-optic data links developed under OMNET feeding a 3-D free-space optical crossbar switch having >Tbps bisection bandwidth.

Develop the key enabling technologies:

- **Heterogeneous integration of large arrays of optoelectronic components.**
- **Low-threshold VCSELs, photodetectors, Si CMOS ICs, micro-optics, and advanced multichip module packaging.**

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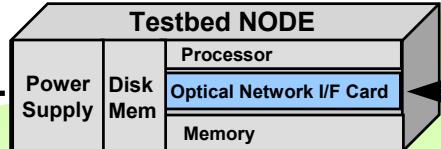
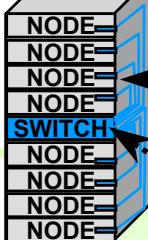
VIVACE VLSI Photonics Program



Hyperspectral Imaging Application Demo



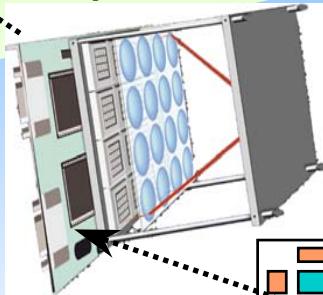
Testbed



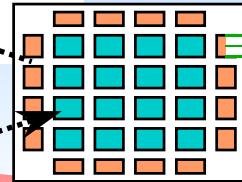
System Demo

Modeling & Simulation

Free-Space Optical Switch



Large-Scale Smart Pixel Array



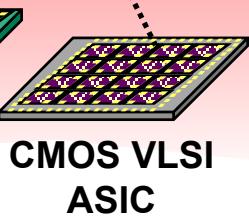
OE-Switch MCM

Integration & Packaging

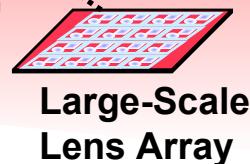
Components



Large-Scale OE 2-D Array



CMOS VLSI ASIC



Large-Scale Lens Array



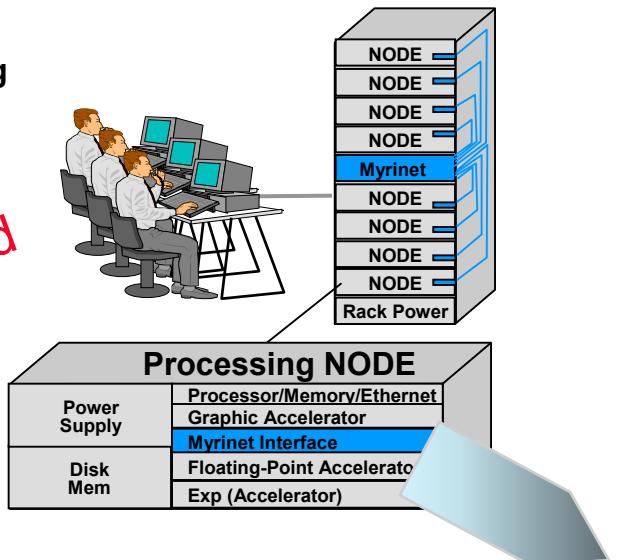
Vivace Demonstrations



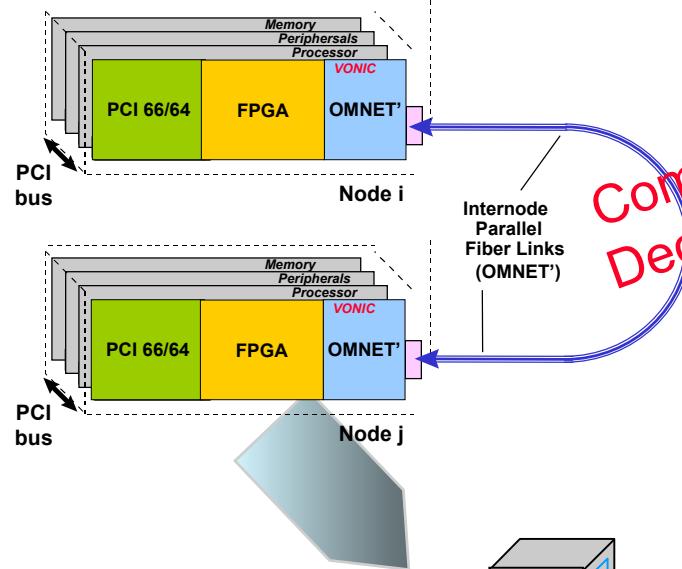
1. System/Application Verification

Boeing
HSI

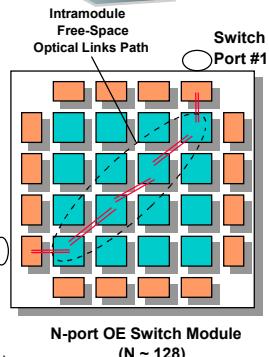
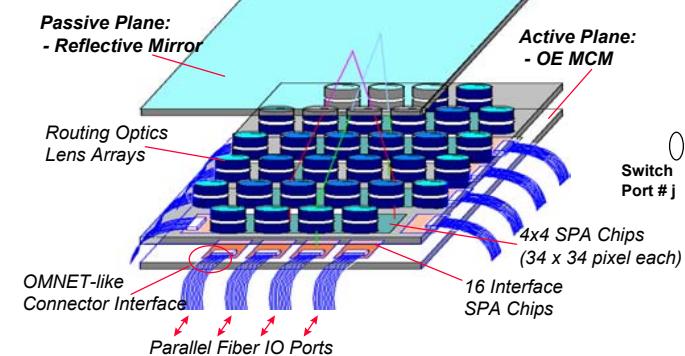
Completed
Dec '99



2. VIVACE Optical NIC (VONIC) and Fiber Link Demo

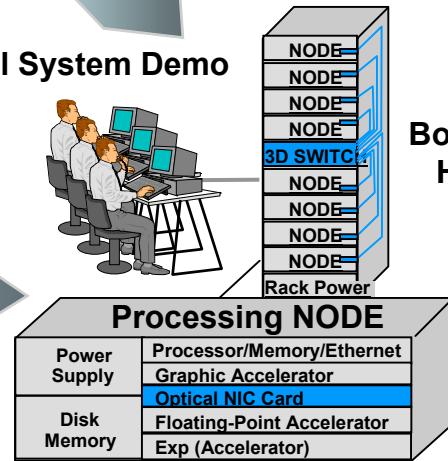


3. Interim 3-D Switch Demo



4. Final System Demo

Boeing
HSI



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VIVACE Test & Demonstration Milestones



| Date | Demo ID | CDRL | Location | Key Feature |
|---------|---------|------|----------|---|
| Jul 99 | 3A | - | AP | FastNet Yr 2 Demo of 3-D switch optics, 8x8 SPAs |
| Dec 99 | 1 | A005 | Fla | System Architecture Verification (Myrinet switch fabric) |
| Jun 00 | 2A | - | UDel | VONIC-OMNET'-VONIC signal integrity (without PCI) |
| Dec 00 | 2 | A006 | UDel | VONIC-OMNET'-VONIC Link Verification (with PCI) |
| May 02* | 3B | - | AP | Verification of final switch optics Small SPAs, final cluster size |
| Jan 02 | 4A | - | HTC | VONIC-OMNET'-VONIC + PCI + MPI |
| Jan 03* | 3 | A007 | AP/UDel | Interim Switch Demo - verification of final ASIC Full sized SPA, fully populated MCM |
| Jan 03* | 4B | - | AP/UDel | VONIC-Switch-VONIC using switch from Demo 3 (greater than the InfiniBand 4X data rate- 8Gbps) |
| May 03* | 4C | - | Fla | Preliminary system demo with simple application |
| Jun 03* | 4D | - | Fla | Simulation of HSI with InfiniBand protocol |
| Jun 03* | 4 | A013 | Fla | Final System Demo with HSI application |

* Revised dates resulting from re-plan

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VIVACE Protocols

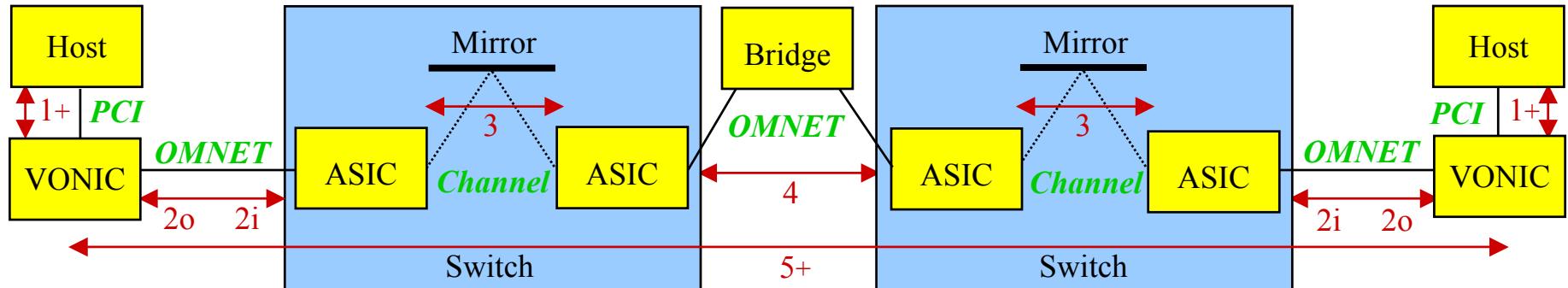


Physical and Data Link layers

Data Link and above layers

} Some overlap of Data Link layers

- 1+. Host–VONIC (Family of Implementation Specific Protocols)
- 2i. VONIC-to-Switch (inbound)
- 2o. Switch-to-VONIC (outbound)
3. Intra-Switch (Channel)
4. Inter-Switch
- 5+. VONIC–VONIC (Family of Implementation Specific Protocols, e.g. MPI or Transparent PCI Extension)



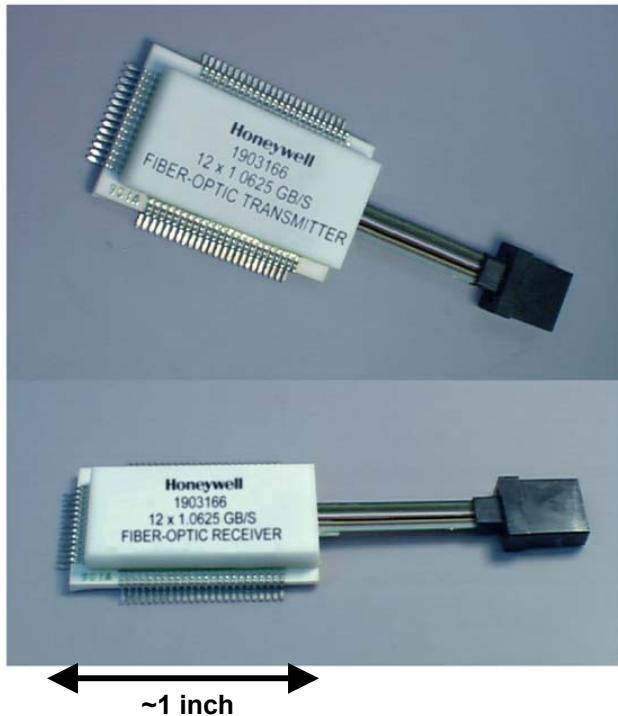
Features

- True Multicast Capability (including subset retries)
- Autonomy (No Shared Control) Allows True Concurrency
- Very Low Message Overhead
- Unlimited Packet Size
- Low Latency
- Efficient Hardware Flow Control
- Efficient Hardware NAKs (Busy and Error)
- Flexible Interface (PCI 64/66 → InfiniBand)
- Supports Multi-Switch Fabrics (Scalability)
- Unlimited Node Address Space

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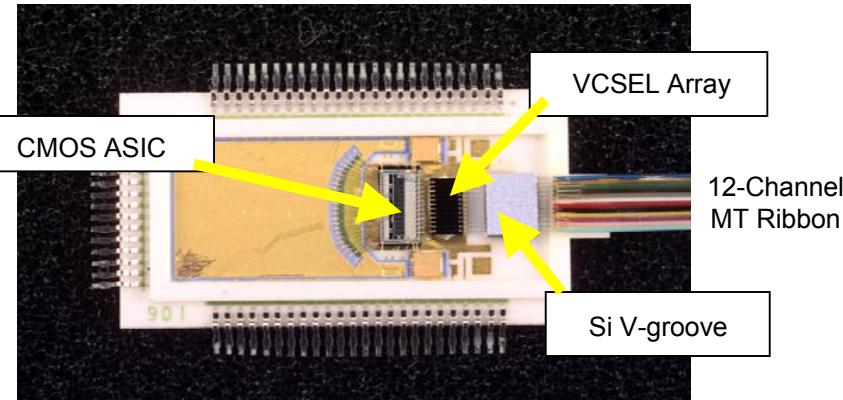


OMNET-Derivative Parallel Optical Data Links for VIVACE



Overview

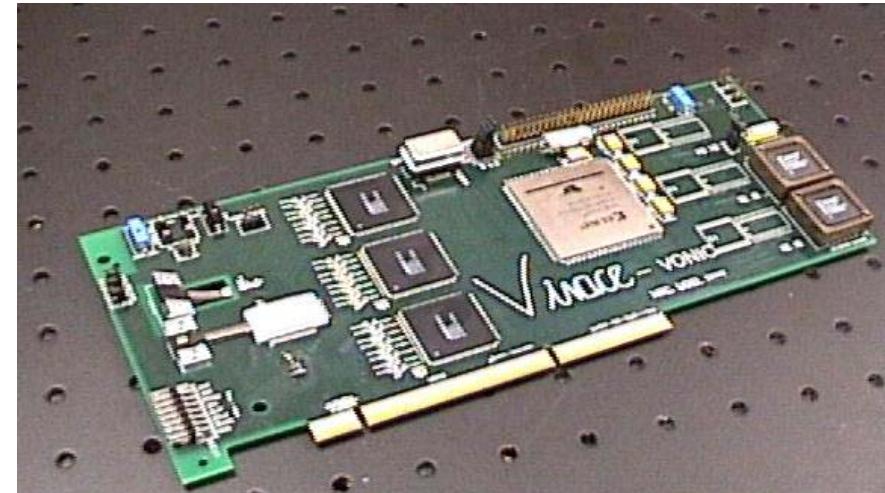
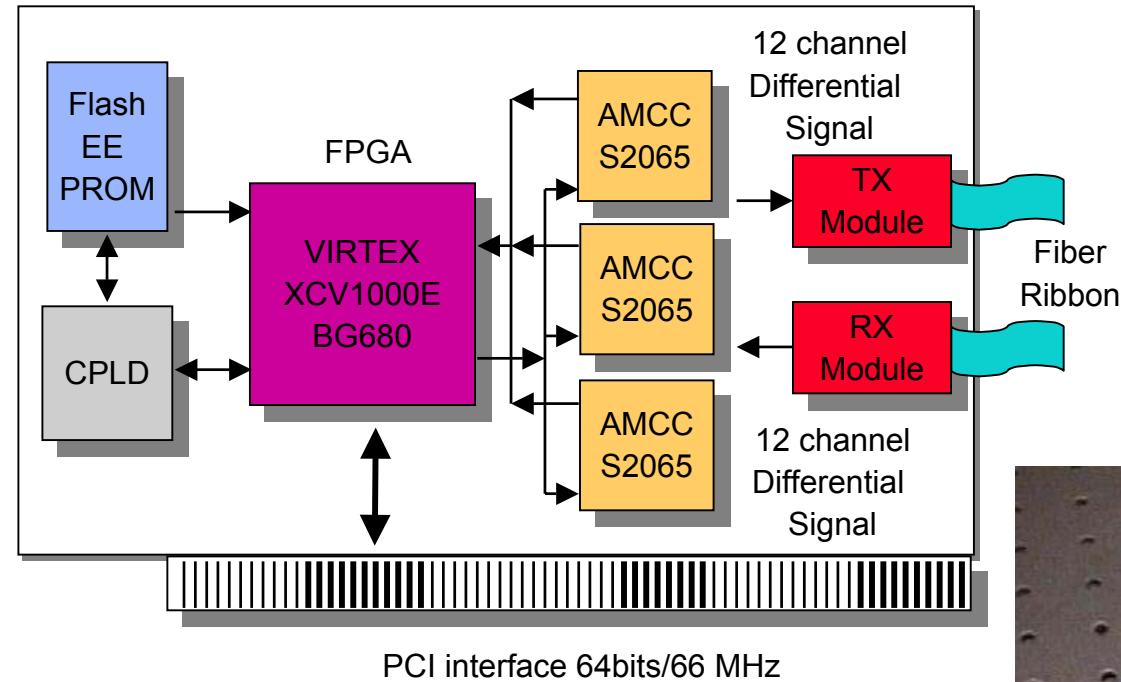
- Internally developed at HTC for ruggedized applications
- Engineering prototypes delivered to potential users for evaluation
- TX module: 1 x 12 array of standard Micro Switch 850-nm VCSELs with Helix HXT 2000 ASIC
- RX module: 1 x 12 array of Micro Switch GaAs PIN detectors with Helix HXR 2012B ASIC
- Silicon V-groove fiber interface with metallized-angle polish
- Low-profile package
- Standard MT connectors, fiber ribbon (250- μ m pitch)
- Tested up to 2 GHz per channel



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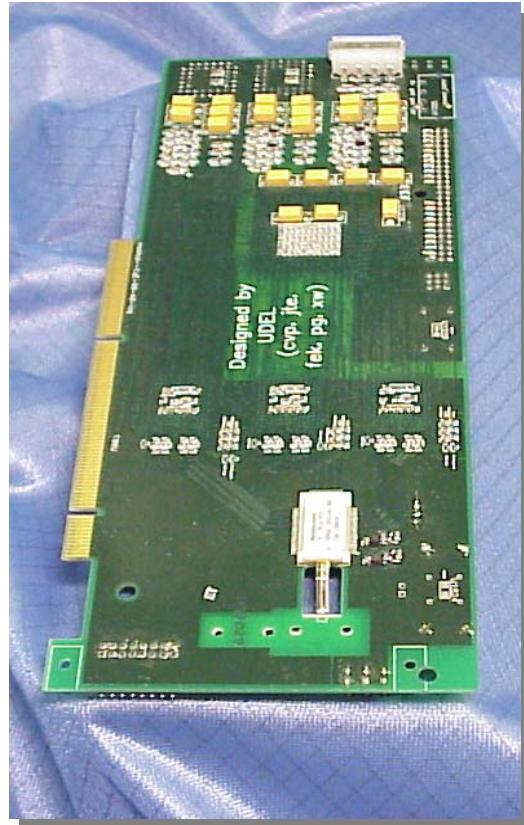
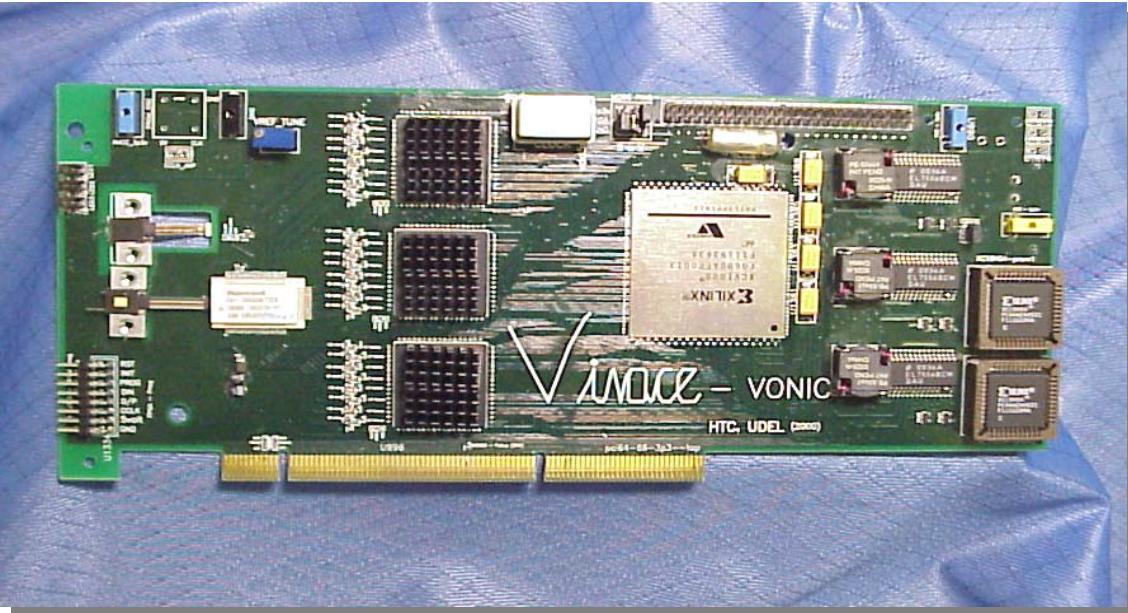
VONIC with PCI 64bit/66MHz Interface



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VIVACE Optical Network Interface Card (VONIC)



Front side / Back side

8 layers
Copper / FR-4

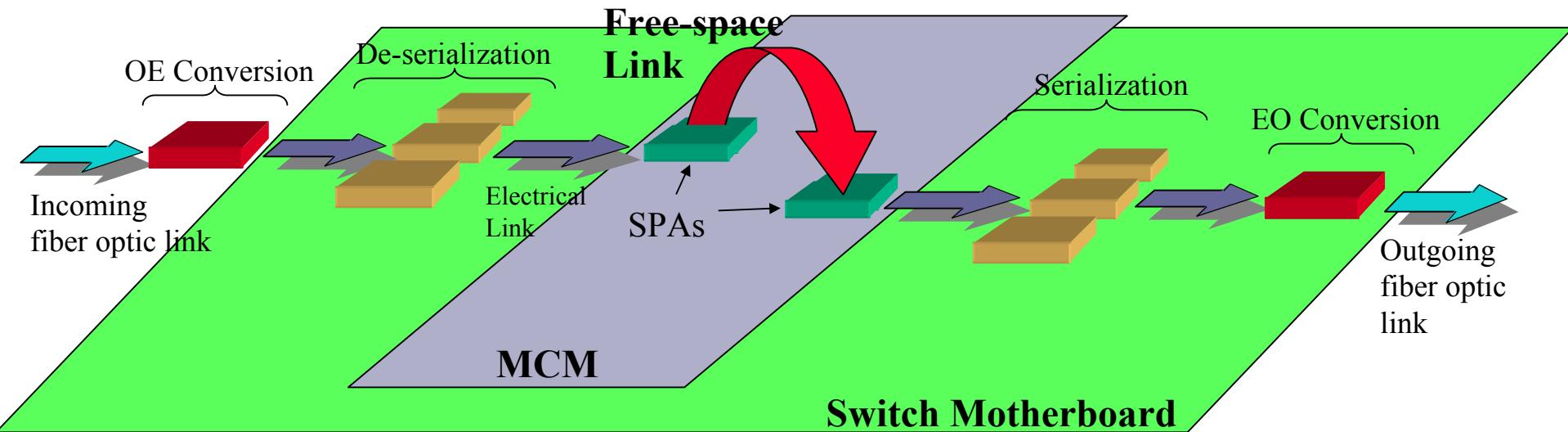
64-bit / 66 MHz PCI
184-pin edge connector

>10 Watt power consumption
5-volt power supply

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VIVACE Multi-Chip Module

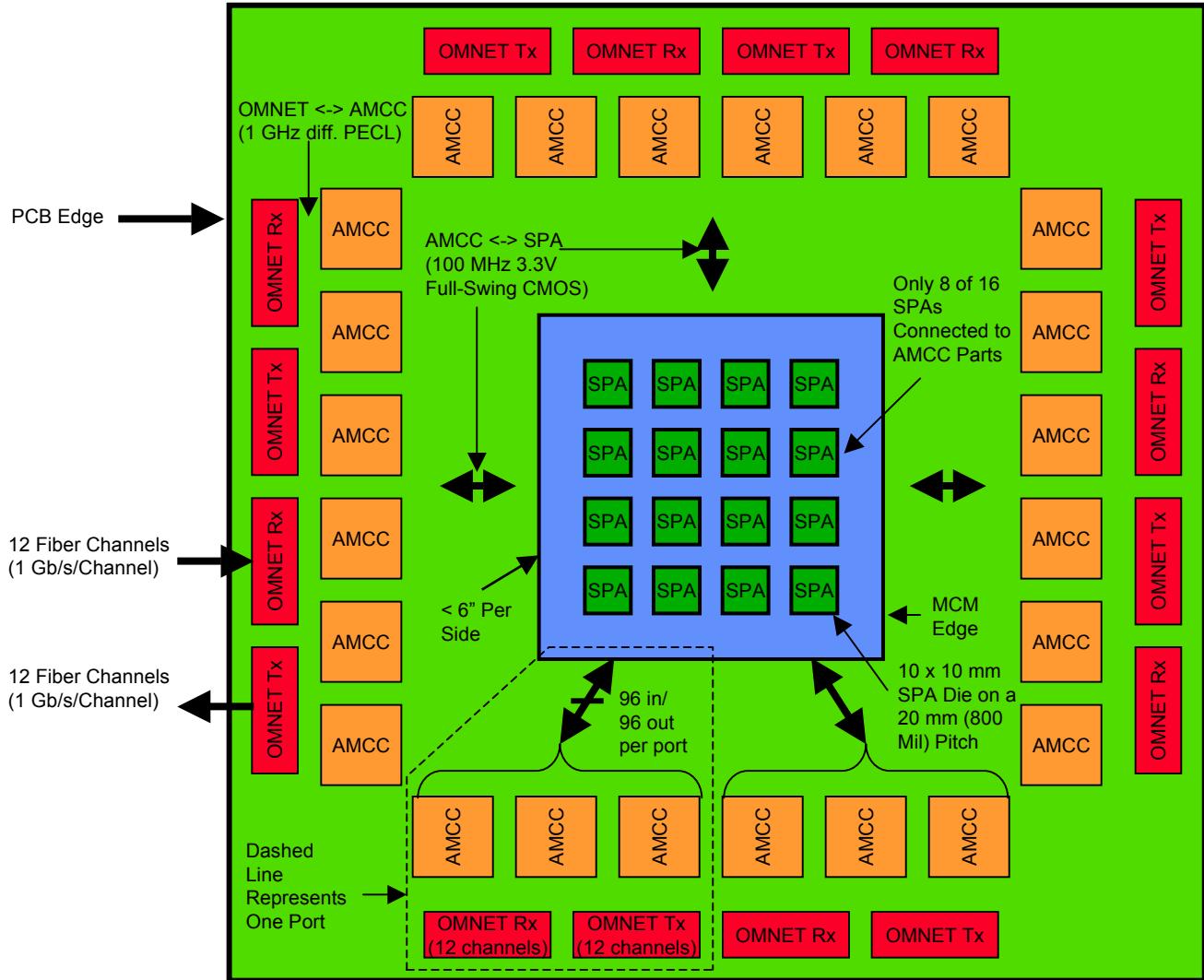


Incoming fiber port from one node to outgoing fiber port to another node
is shown

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Switch MCM



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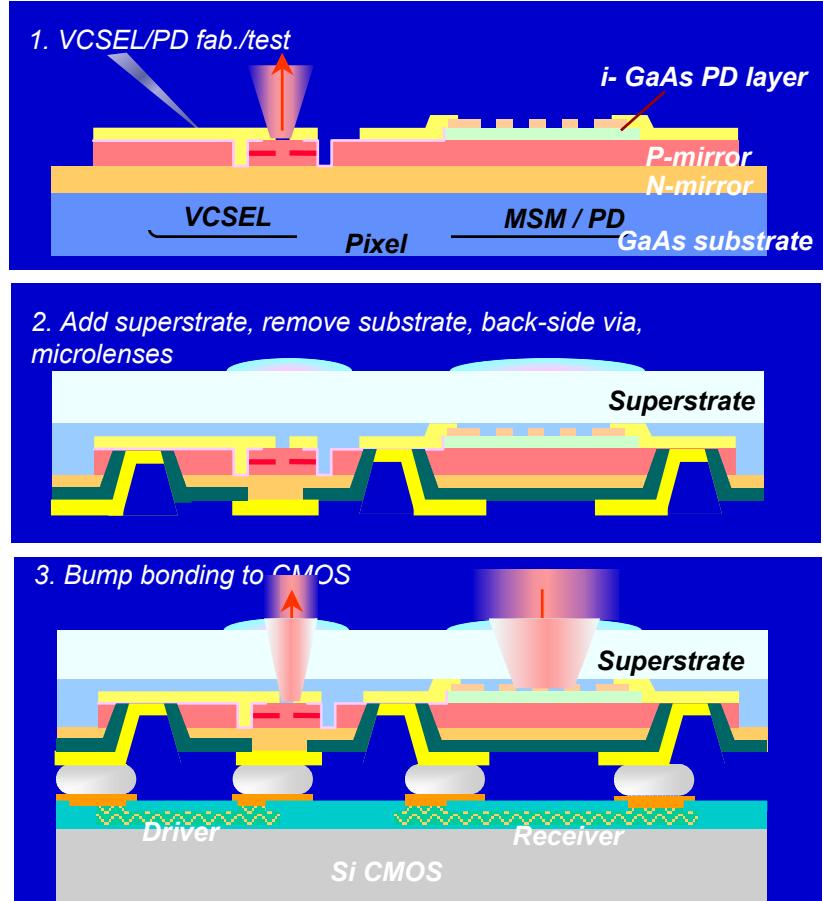


Our Smart Pixel Array Integration Approach



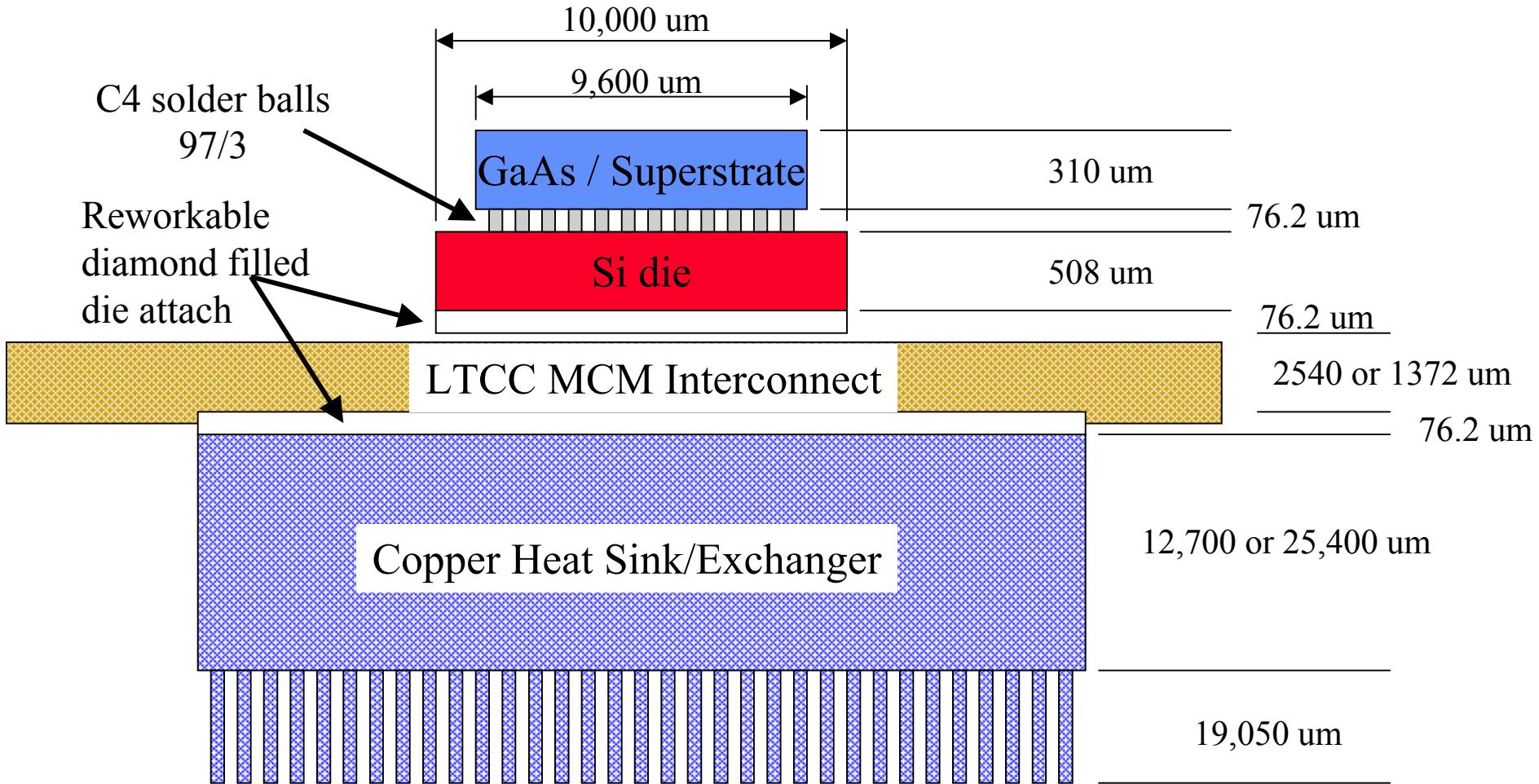
Emphasis on Producibility:

- **Based on 850-nm top-emitting VCSEL with integrated MSM:**
 - Built on existing processes
 - Allows **wafer-scale** device testing and screening **before** any further integration!
- **Transparent superstrate:**
 - Provides rigid carrier for **wafer-scale** backside processing (thinning, via)
 - Allows micro-optics integration and evaluation done on the **wafer scale**
- **Chip-scale bump-bonding to Si IC:**
 - Standard bump-bonding process
 - Backside metal provides additional routing and bonding flexibility
 - All devices are visible from top for easy inspection and testing





Assembly Side View



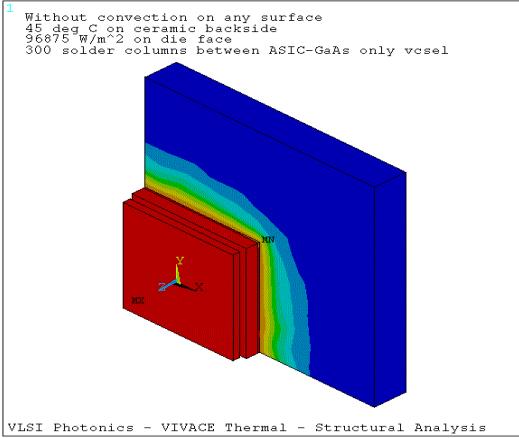
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ANSYS Sequential Thermal-Stress Analysis

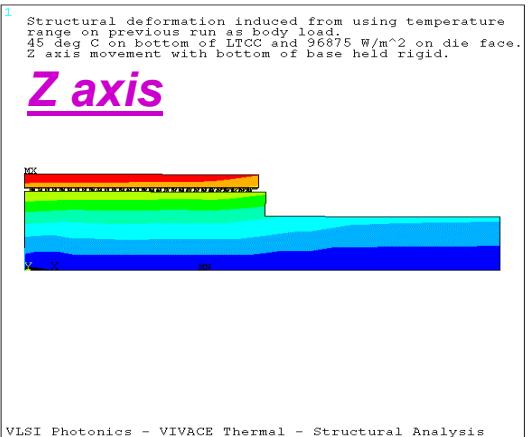


Thermal analysis temperature profile



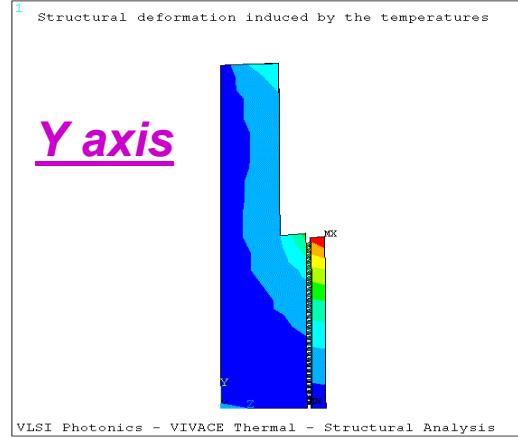
Temp.
In °C

Structural analysis from induced temp



Movement
In meters

Structural analysis from induced temp

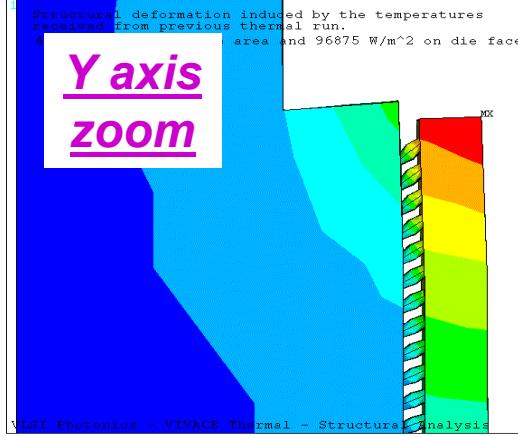


Y axis

ANSYS 5.6.2
FEB 8 2001
20:02:51
NODAL SOLUTION
STEP=1
SUB=1
TIME=1
UY (AVG)
RSYS=0
Power-Graphics
EFACET=1
AVRES=All
DMX =.239E-05
SMN =-.463E-07
SMX =.921E-06
XV =-1
DIST=.006345
XF =.005249
YF =.005537
ZF =.001278
Z-BUFFER
-.463E-07
.612E-07
.726E-06
.384E-06
.491E-06
.539E-06
.656E-06
.813E-06
.921E-06

Movement
In meters

Structural analysis from induced temp

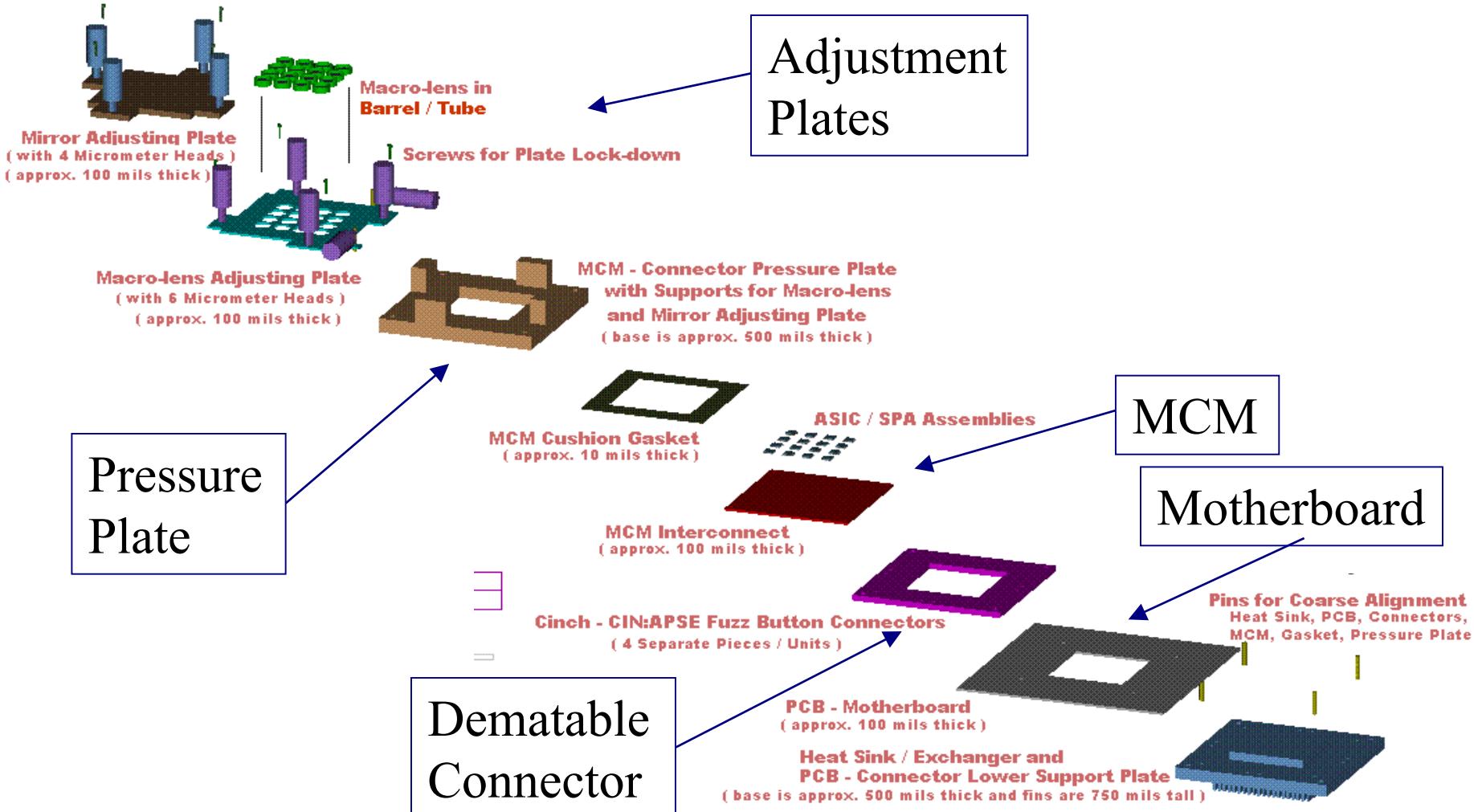


Movement
In meters

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Mechanical Assembly Components



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Packaging Challenges



FAST-Net

- 6.6 mm, 0.5 μm ASIC
- 6 SPAs placed on MCM
- 4-bit links between SPAs
- MCM-L substrate
 - 4.0 x 3.8 inch
 - 6 layers
 - 140 MCM interconnect
- Interface through 152-pin Mictor connector
- Power consumption not an issue

VIVACE

- 10 mm, 0.25 μm ASIC
- 16 SPAs per MCM
- 44-bit links between SPAs
- MCM-C substrate
 - 5.0 x 5.0 inch
 - 16 layers
 - 2000 MCM interconnect
- Interface through 4000-pin fuzz-button connector
- > 160 Watts power consumption possible

VIVACE packaging approach must be closely considered!

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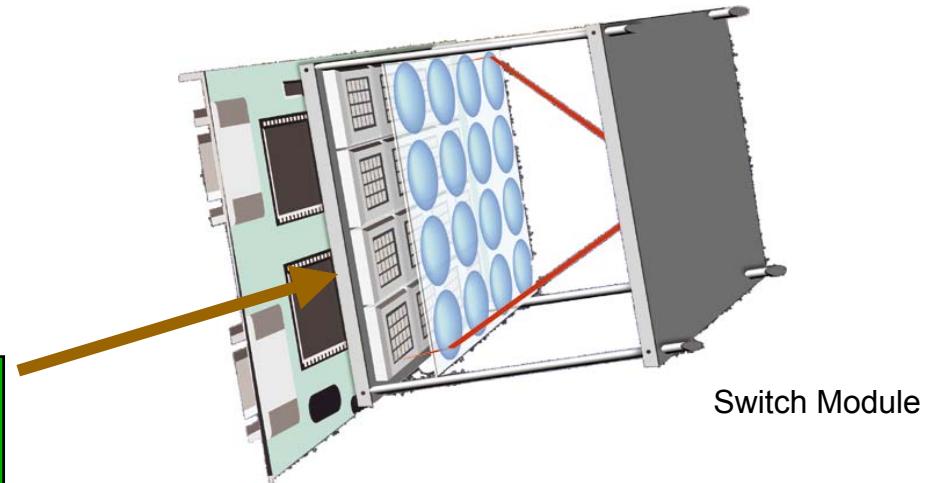
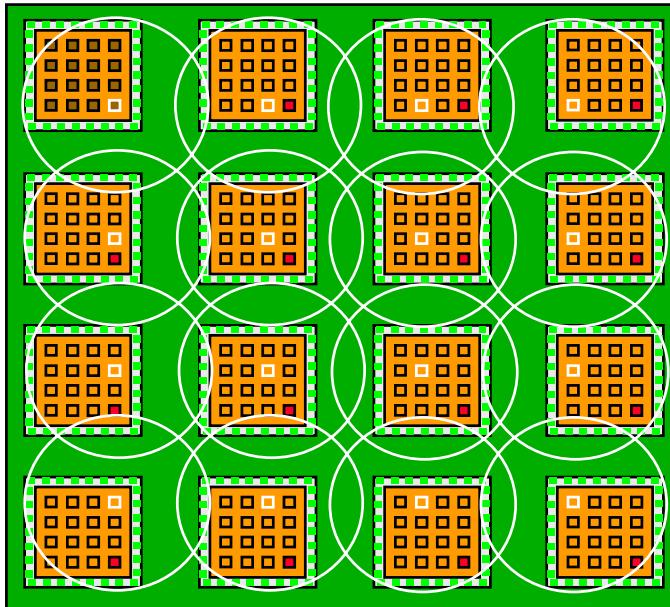


VIVACE 3-D Free-Space Switch Approach



Key Features

16 x 16 Crossbar
MCM with 4 x 4 SPAs
~5 Tbps BSBW

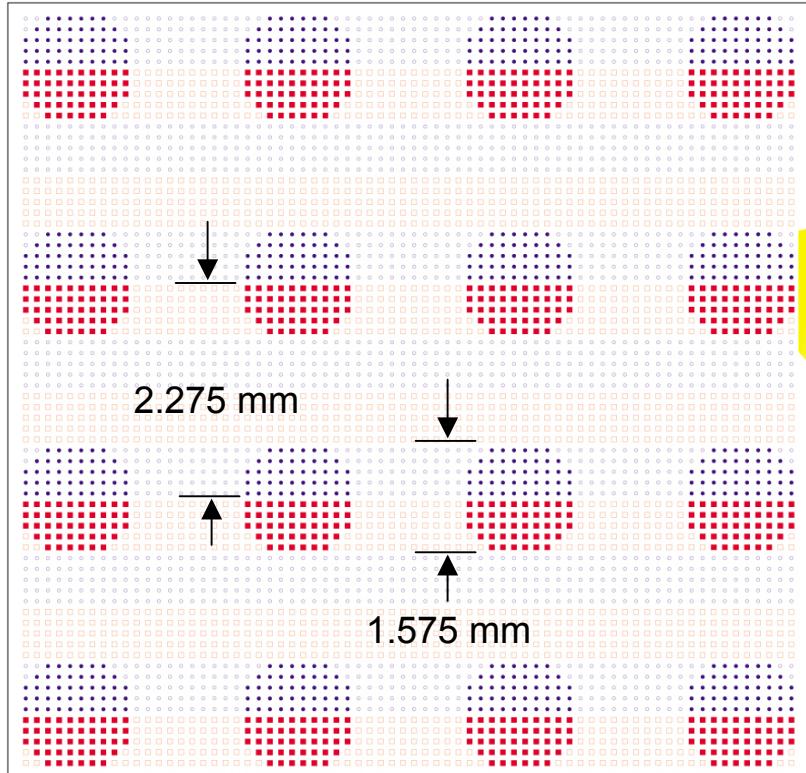


- Optical system must create 11,264 links across a 5 inch MCM with sub-60 micron resolution and registration!

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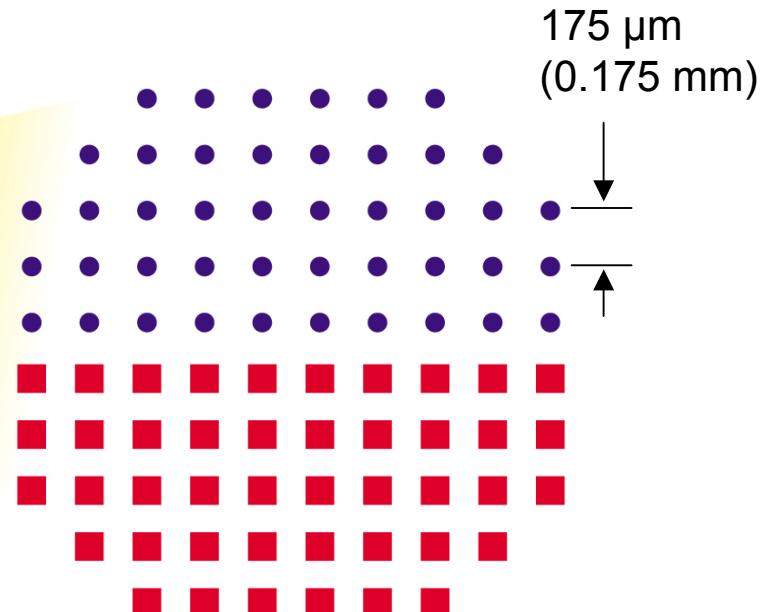


New Switch SPA Chip Layout



Switch Chip

- O/E devices bonded out in clusters to provide self-similarity
- 44 VCSELs ($NA \approx 0.26$)
- 44 PDs (60 μm side)



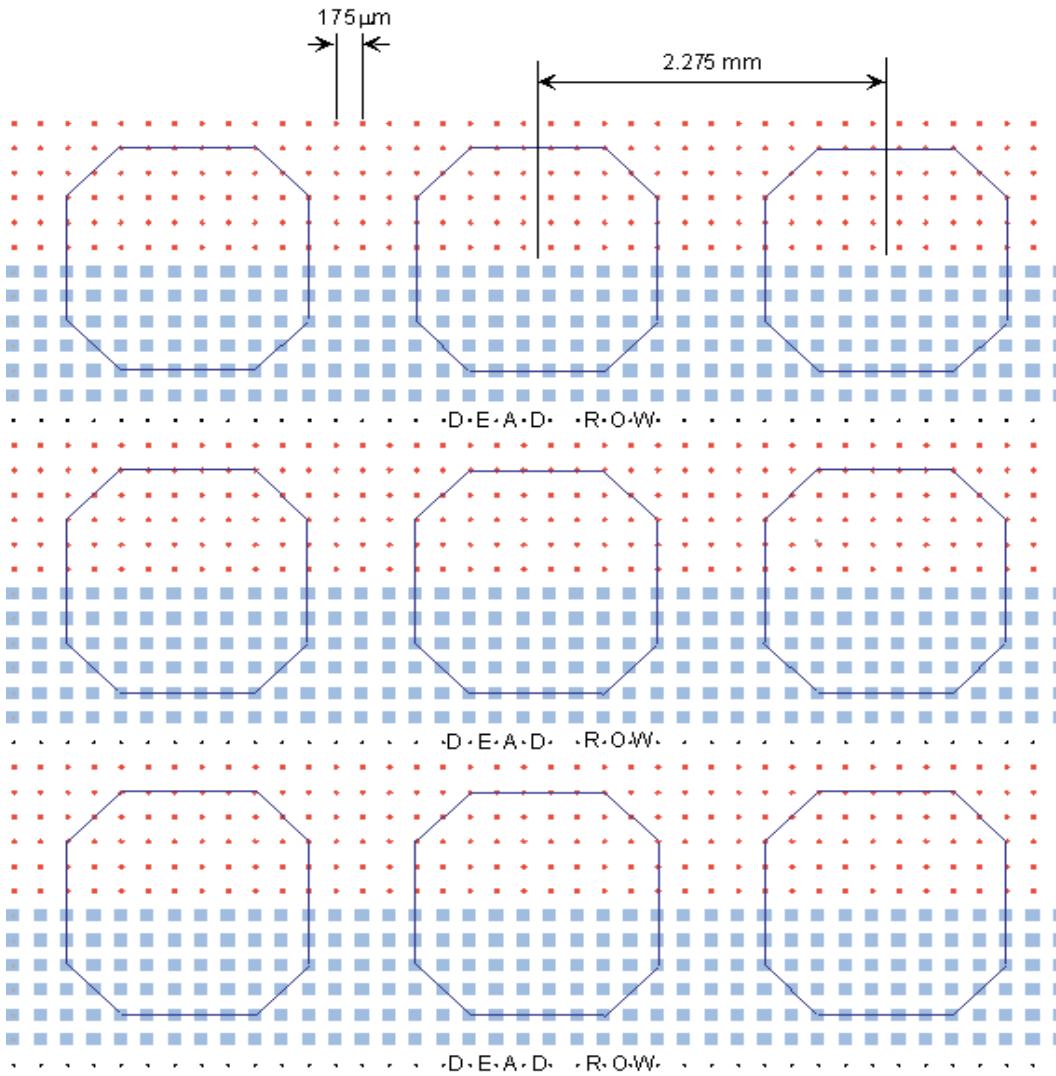
Cluster Configuration

- 32 - data
- 1 - control
- 11 - redundancy
- In “test mode”, all 44 are used

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NEW CHIP LAYOUT

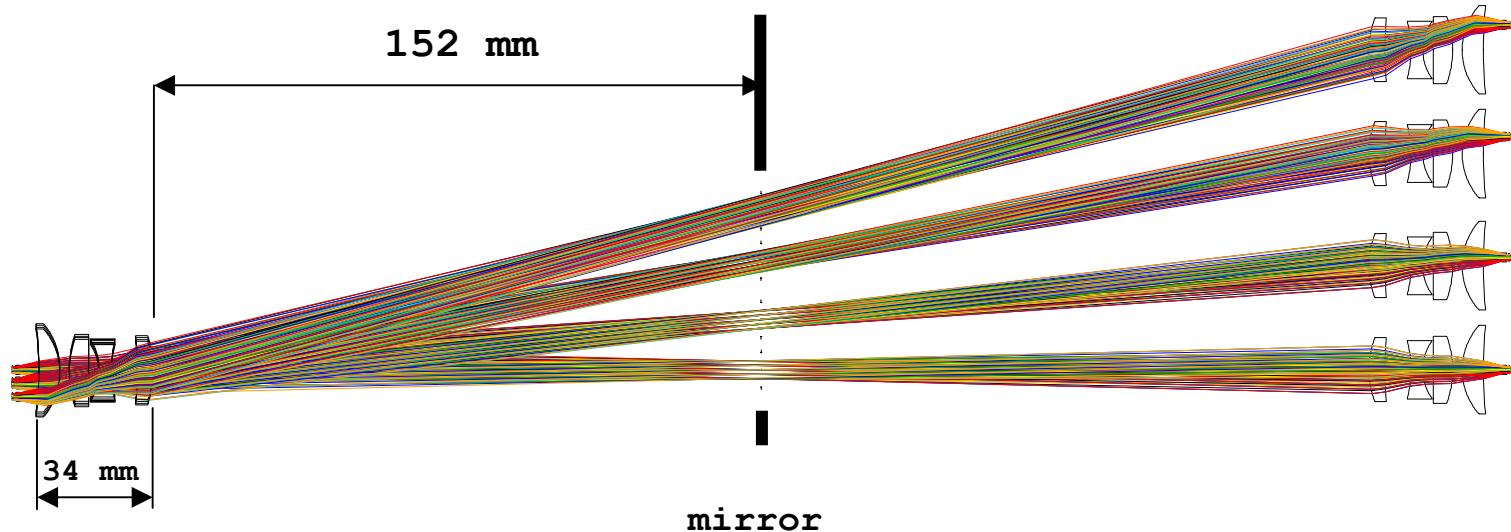


- Full mask should comprise all 16 clusters plus some edge margin.
- Clusters are shown as dark blue octagons.
- Detector is 60 μm side.
- The pattern is: 6 rows of VCSELs, 6 rows of detectors and one undefined “dead” row
- Using over 50% of all VCSELs/PDs.

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CROSS SECTION OF THE *VIVACE* OPTICS



- For performance/cost reasons system lengthened.
- Aspect ratio ~ 1.3

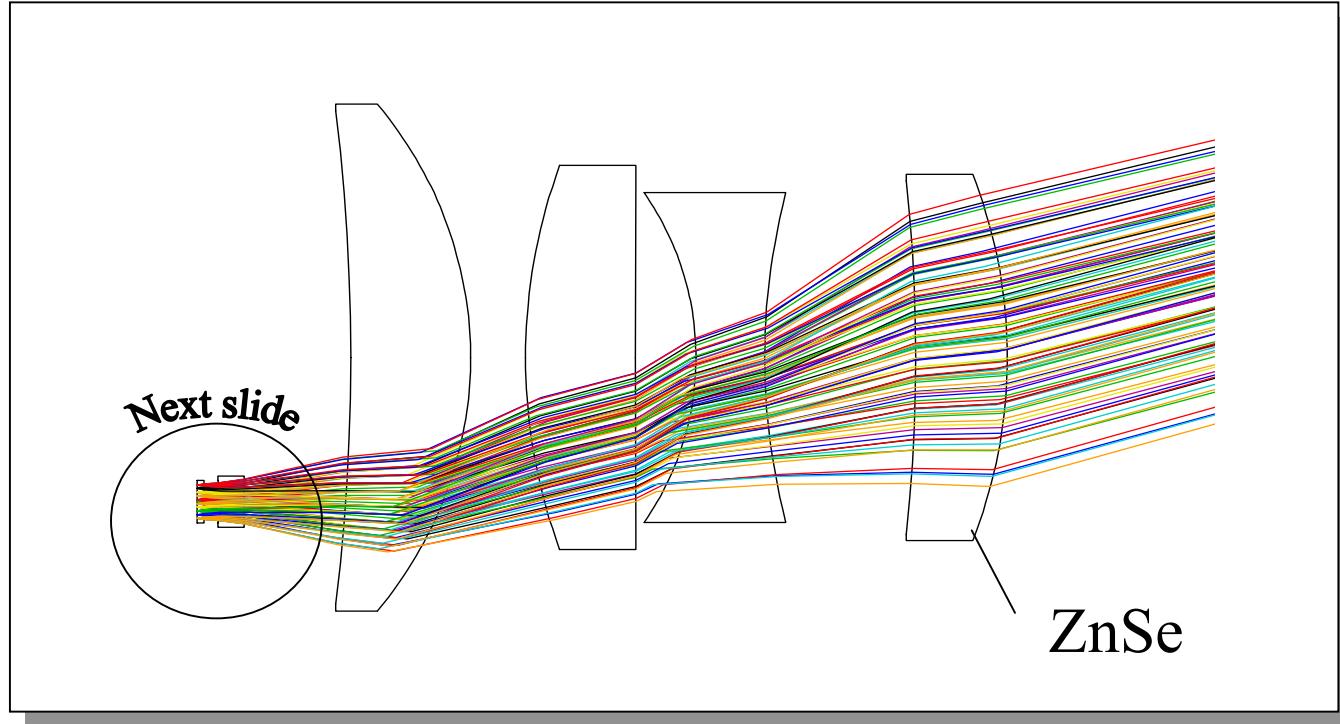
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FINAL LENS DESIGN cont'd



Hybrid *micro–mini–macro* lens implementation.

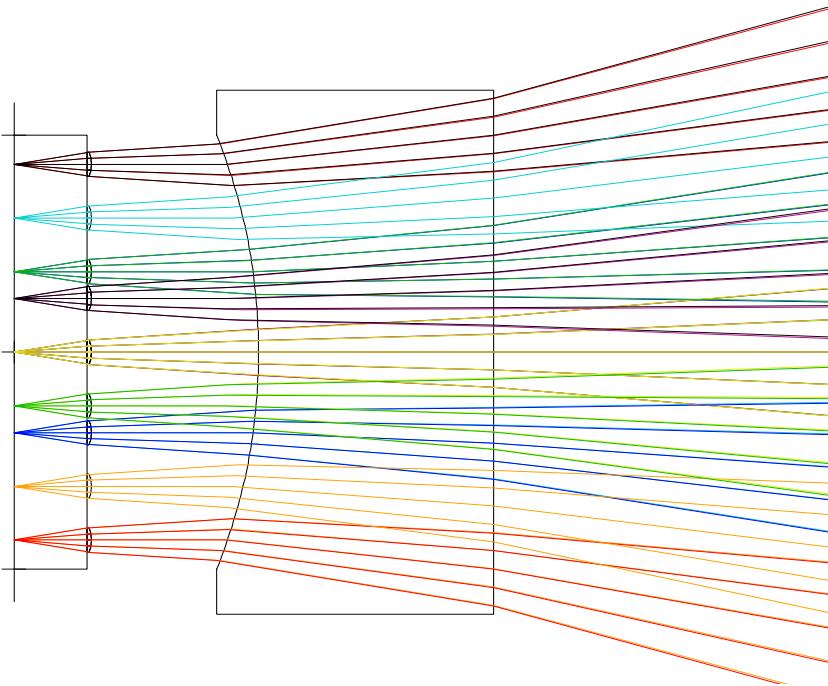


- Macro-lens is 4-element double-Gauss all-spherical lens.
- Diameter is 29 mm max (with the barrel).

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MINI AND MICRO LENSES



- Micro lens diameter: 150 μm .
- Mini-lens diameter: 2 mm.

- Micro-lenses reduce the VCSEL NA by the factor of 4.
- Mini-lenses are plano-concave; they steer the VCSEL beams to remove distortion and do some aberration control; concave surface is the only aspherical surface in the system.
- Combination of Macro-Mini-Micro affords 0.05% distortion at full field
- The *VIVACE* lens, although very complex, is manufacturable!

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